ABSTRACT

In one embodiment, the present invention is directed to a method of designing an application specific integrated circuit (ASIC). The method comprises (a) performing static timing analysis on versions of an ASIC design multiple times before routing the ASIC design utilizing path delays that are estimated according to cardinality of fanout of nets of the ASIC design and (b) performing static timing analysis on versions of the ASIC design multiple times before routing the ASIC design utilizing path delays that are calculated from estimated routing distances within a current version of the ASIC design, wherein step (a) is performed more frequently than step (b).